1. Synthesis Result:

Graphical user interface, diagram

Description automatically generated

Figure-7: Synthesis Result of Memory Design

1. Graphical user interface

   Description automatically generated with medium confidenceVerification and Analysis:

Figure-8: Functional Simulation waveform of the Memory Design

1. In the memory design, 7 bit address is taken as the memory contains total of 128 words. In the functional simulation of the memory design, random data\_in value of 8 bits were written in a random address 0100000 when there is positive clock edge in the clock signal. In figure 8, we appropriate result of read and write is achieved as per the logic of VHDL code written for this design. At the very beginning, since it did not satisfy any of the condition in positive clock edge so, arbitrary value 00000000 is shown in data\_out. Again, in positive clock edge, when write enable (WE) is high and read enable(RE) is low then it writes 01110101 to the address and in next positive clock edge when WE is low and RE is high it reads from the same address in data\_out. So, data\_out shows 01110101 as output. If neither of the condition is satisfied so it holds the previous value in the data\_out which matches according to the code. Since it is functional simulation there is no time delay in output.

b.

Graphical user interface

Description automatically generated with medium confidence

Figure-9: Timing Simulation waveform of the Memory Design

In case of timing simulation, the end time of the simulation is increased to 40ns from 20ns so that data\_out value is visible after reading is completed. In figure 9, it reads the value 01101101 from 1011011 address. There is a reading delay of 29.102-19.01= 10.092ns to show the value of 01101101 in data\_out.